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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,594	05/16/2001	Toyohiko Yoshida	57454-116	9350

7590 06/03/2004

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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	3

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,594	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been examined.

Papers Received

2. Receipt is acknowledged of Information Disclosure Statement paper submitted, where the paper has been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 16 May 2001 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner, however, only to the extent possible through the translated portions since the examiner does not understand Japanese.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-9 and 14-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claims refer to a memory operation unit, a piece of hardware, as "generating a pipeline stage." A pipeline stage is taken to be actual hardware in the art. One of ordinary skill in the art would not recognize how hardware could create other hardware. The only possibility would be if the device were implemented on an FPGA or

other such programmable logic, however, the specification does not give this as the case. Likewise, there is no description of how the pipeline stages are being generated by hardware in the specification, but only that it is being done. Therefore, one of ordinary skill in the art would not be enabled without undue experimentation to make and use the invention. The examiner is interpreting the claims to actually mean that hardware is "generating a pipeline cycle," that is control is established by the hardware to process for a cycle. The examiner is then taking the limitations that include "without generating a pipeline stage" to mean that an extra cycle is not generated in addition to the already generated cycle.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-9 and 10-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claims 1, 3, 4, 7, 14, and 16 state that a memory operation unit is generating a pipeline stage for some functionality and claims 3 and 7 state that a memory operation unit is not generating a pipeline stage for some other functionality. A pipeline stage is taken to be actual hardware in the art. One of ordinary skill in the art would not recognize how hardware could create other hardware. The only possibility would be if the device were implemented on an FPGA or other such programmable logic, however, the specification does not give this as the case. The examiner is interpreting the claims to actually mean that hardware is "generating a pipeline cycle," that is control is

established by the hardware to process for a cycle. The examiner is then taking the limitations that include "without generating a pipeline stage" to mean that an extra cycle is not generated in addition to the already generated cycle. Clarification on this manner is required.

9. Claim 10 recites the limitation "said dedicated register" in lines 15-16. There is insufficient antecedent basis for this limitation in the claim. A register has been defined as retaining an instruction but it has not been named the dedicated register. The examiner is taking the claim to mean "said register."

Claim Objections

10. Claim 10 is objected to because of the following informalities: The last limitation in the claim is unclear in regard to the register in the register file and its role in the system. The examiner is taking the limitation to read, "said memory operation unit retaining, in a register in said register file, an instruction in a loop of instructions corresponding to a repeat instruction when said repeat instruction is executed, and executing the loop of instructions while fetching an instruction retained in said register," so that it is clear that the instruction from the loop is being retained in the register of the register file where it is then fetched for execution as stated in the specification. Also, line 6 states the limitation "connected to an instruction memory" however an instruction memory has already been defined. The examiner is taking the claim to mean "connected to the instruction memory" to show that the same instruction memory is meant as is the case in the specification. Similar problems exist with limitations in claims 11-13 and the same interpretation is being taken by the examiner.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Okado (EP 0 511 484 A2).

13. In regard to claim 10, Okado discloses a data processing apparatus comprising:

a. an instruction memory in which an instruction is stored (figure 1, element 201); Column 9, lines 4-8 show that this ROM is a program or instruction memory.

b. a data memory in which data is stored (figure 1, element 101);

c. an instruction decoder decoding a fetched instruction (figure 1, IDEC);

d. a register file (figure 1, IR1 and IR2);

e. a memory operation unit (figure 1, elements 103 and 207) connected to the instruction memory, said data memory and said instruction decoder, fetching an instruction stored in said instruction memory, and accessing said data memory according to a decoded result of said instruction decoder; Column 10, lines 12-15 show that the repeat controller portion allows instructions to be read (fetched) from the micro ROM (instruction memory). Figure 1 shows that the a

the pointer portion is used to access the data memory based on the decoder output on line 202.

f. and an integer operation unit carrying out an integer operation according to a decoded result of said instruction decoder; Figure 1 shows ALU 1, which performs arithmetic functions and is an integer unit. Notice the outputs 204 of the decoder. Column 9, lines 28-31 show that this output of the decoder controls the arithmetic logic operations.

g. said memory operation unit retaining, in a register in said register file, an instruction in a loop of instructions corresponding to a repeat instruction when said repeat instruction is executed, and executing the loop of instructions while fetching an instruction retained in said dedicated register. Column 9, line 35 – column 10, lines 48 details how the repeat controller (part of the memory operation unit) stores one or more repeat instructions in instruction registers so that when executing a repeat loop the instructions are fetched from the registers instead of memory.

14. In regard to claim 11, Okado discloses the data processing apparatus according to claim 10, wherein said register file comprises a processor status word,

a. wherein said memory operation unit sets a flag in said processor status word at a first execution cycle of said loop, and retains, in the register of said register file, the instruction in the loop of instructions fetched from said instruction memory when said repeat instruction is executed; As shown above, on first execution of a loop, instructions of the loop are retained in the registers IR1 and

IR2 after fetching from memory. This section shows how the repeat controller has an internal state (or processor status flag) to cause fetching from memory or the registers. So when the fetching is done from the memory, the processor status flag is set to do so. Since a word is just a number of bits that a processor can control or operate on, the processor status flag is a processor status word.

b. and resets said flag in said processor status word at a second execution cycle of said loop, and executes said loop while fetching the instruction retained in said dedicated register. When the fetching is done from the registers, the processor status word is reset or set to fetch from these registers.

15. In regard to claim 12, Okado discloses the data processing apparatus according to claim 10, wherein said memory operation unit retains a plurality of instructions in the loop of instructions, when said repeat instruction, in a plurality of registers in said register file, and executes said loop while fetching said plurality of instructions retained in said plurality of dedicated registers. Column 10, lines 33-48 show that a plurality of instructions may be repeated and fetched from a plurality of registers.

16. In regard to claim 13, Okado discloses the data processing apparatus according to claim 12, wherein said register file includes a processor status word, wherein said memory operation unit sets a flag in said processor status word at a first execution cycle of said loop, and retains the plurality of instructions in the loop of fetched from said instruction memory in said plurality of registers, and resets said flag in said processor status word at a second execution cycle of said loop, and executes said loop while fetching said plurality of instructions retained in said plurality of dedicated registers. As

shown above, multiple instructions may be retained and there is a processor status word that flags to fetch instructions from memory and upon doing so and retaining them for future fetching from the registers, the status is reset.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 1-9 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okado in view of Hennessy (Computer Architecture).

19. In regard to claim 1,

a. Okado discloses a data processing apparatus comprising:

i. an instruction memory in which an instruction is stored (figure 1, element 201); Column 9, lines 4-8 show that this ROM is a program or instruction memory.

ii. a data memory in which data is stored (figure 1, element 101);

iii. an instruction decoder decoding a fetched instruction (figure 1, IDEC);

iv. a memory operation unit (figure 1, elements 103 and 207) connected to said instruction memory, said data memory and said instruction decoder, fetching an instruction stored in said instruction memory, and accessing said data memory according to a decode result of

said instruction decoder; Column 10, lines 12-15 show that the repeat controller portion allows instructions to be read (fetched) from the micro ROM (instruction memory). Figure 1 shows that the a the pointer portion is used to access the data memory based on the decoder output on line 202.

v. and an integer operation unit carrying out an integer operation according to a decode result of said instruction decoder; Figure 1 shows ALU 1, which performs arithmetic functions and is an integer unit. Notice the outputs 204 of the decoder. Column 9, lines 28-31 show that this output of the decoder controls the arithmetic logic operations.

b. Okado does not disclose

vi. said instruction memory including a plurality of instruction memory banks;

vii. said memory operation unit generating a pipeline stage corresponding to selection of an instruction memory bank and a pipeline stage corresponding to instruction readout to carry out pipeline processing when a plurality of instructions are fetched from a plurality of said instruction memory banks.

c. Hennessy has disclosed on pages 361-363 the use of memory banks for memory systems. Page 362 shows that one memory bank initiation or read is completed per clock cycle. The pages show that when reading from multiple

banks, one bank is read from while the other is then selected in a generated cycle so that in the next generated cycle that bank is read from.

d. Page 361 of Hennessy shows that multiple memory banks allow for producing or accepting one word fetched or stored per clock cycle, which is faster than using one memory bank. This ability to speed up memory transfers would have motivated one of ordinary skill in the art to modify the design of Okado to use multiple memory banks in the instruction memory.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Okado to implement a plurality of memory banks in the instruction memory system as taught by Hennessy so that transfers of the memory are sped up.

20. In regard to claim 2, Okado in view of Hennessy discloses the data processing apparatus according to claim 1, wherein said instruction memory further includes a first bank select circuit decoding an address including a low order address to generate chip select signals of said plurality of instruction memory banks so that a different instruction memory bank of said plurality of instruction memory banks is accessed when instructions at continuous addresses are accessed. It is inherent that if two instructions are stored at two memory addresses separated by the border of memory banks, that the memory bank must be switched to access the second instruction and that the low order address would play a role in chip-selecting the bank since it gives the border address of the bank.

21. In regard to claim 3,

a. Okado in view of Hennessy discloses the data processing apparatus according to claim 1,

b. Okado in view of Hennessy as applied above does not disclose wherein said instruction memory further includes a high speed instruction memory, wherein said memory operation unit generates a pipeline cycle corresponding to instruction readout to carry out a pipeline process without generating a pipeline stage corresponding to selection of an instruction memory bank when fetching an instruction from said high speed instruction memory.

c. Hennessy has disclosed on pages 18-20 the concept of caches in the memory hierarchy. The cache does not have memory banks and thus does not require a cycle to select a bank. A cache is a fast or high-speed memory.

d. Hennessy has shown that a cache is a fast or high-speed local memory for holding commonly used information. The ability to have a fast memory to fetch instructions from would have motivated one of ordinary skill in the art to modify the design of Okado in view of Hennessy as applied above to include an instruction cache.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Okado in view of Hennessy as applied to above to include a cache as taught by Hennessy for storing instructions so that instructions may be fetched quicker.

22. In regard to claim 4,

a. Okado in view of Hennessy discloses the data processing apparatus according to claim 1,

b. Okado in view of Hennessy does not disclose wherein said data memory includes a plurality of data memory banks, wherein said memory operation unit generates a pipeline stage corresponding to selection of a data memory bank and a pipeline stage corresponding to data access to carry out a pipeline process when accessing said plurality of data memory banks.

c. Hennessy has disclosed on pages 361-363 the use of memory banks for memory systems. Page 362 shows that one memory bank initiation or read is completed per clock cycle. The pages show that when reading from multiple banks, one bank is read from while the other is then selected in a generated cycle so that in the next generated cycle that bank is read from.

d. Page 361 of Hennessy shows that multiple memory banks allow for producing or accepting one word fetched or stored per clock cycle, which is faster than using one memory bank. This ability to speed up memory transfers would have motivated one of ordinary skill in the art to modify the design of Okado in view of Hennessy to use multiple memory banks in the data memory.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Okado in view of Hennessy to implement a plurality of memory banks in the data memory system as taught by Hennessy so that transfers of the memory are sped up.

23. In regard to claim 5, Okado in view of Hennessy discloses the data processing apparatus according to claim 4, wherein said data memory further includes a second bank select circuit decoding an address including a high order address to generate chip select signals of said plurality of data memory banks in order to divide said plurality of data memory banks into two different regions. It is inherent that a higher order address will divide a memory bank into two sections. The highest bit of a memory address that switches within a memory bank indicates two section of that bank.

24. In regard to claim 6, Okado in view of Hennessy discloses the data processing apparatus according to claim 5, wherein said second bank select circuit decodes an address including a low order address to generate chip select signals of said plurality of data memory banks so that a different data memory bank in said plurality of data memory banks is accessed when data at continuous addresses in said two different regions are accessed. It is inherent that if two instructions are stored at two memory addresses separated by the border of memory banks, that the memory bank must be switched to access the second instruction and that the low order address would play a role in chip-selecting the bank since it gives the border address of the bank.

25. In regard to claim 7,

a. Okado in view of Hennessy discloses the data processing apparatus according to claim 4,

b. Okado in view of Hennessy does not disclose wherein said data memory further includes a high speed data memory, wherein said memory operation unit generates a pipeline stage corresponding to data access to carry out a pipeline

process without generating a pipeline stage corresponding to selection of a data memory bank when accessing said high speed data memory.

c. Hennessy has disclosed on pages 18-20 the concept of caches in the memory hierarchy. The cache does not have memory banks and thus does not require a cycle to select a bank. A cache is a fast or high-speed memory.

d. Hennessy has shown that a cache is a fast or high-speed local memory for holding commonly used information. The ability to have a fast memory to retrieve data from would have motivated one of ordinary skill in the art to modify the design of Okado in view of Hennessy as applied above to include a data cache.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Okado in view of Hennessy as applied to above to include a cache as taught by Hennessy for storing instructions so that data may be retrieved quicker.

26. In regard to claim 8, Okado in view of Hennessy discloses the data processing apparatus according to claim 1, wherein said memory operation unit fetches an instruction from said instruction memory via an instruction bus (Okado, figure 1, line from element 201 to IR1) and accesses said data memory via a data bus (figure 1, element 106) differing from said instruction bus.

27. In regard to claim 9, Okado in view of Hennessy discloses the data processing apparatus according to claim 1, wherein said memory operation unit reads out data from said data memory via a data input bus, and writes data into said data memory via a data output bus differing from said data input bus. Figure 1 of Okado shows that there is a

bus that inputs data to the data memory and a separate bus that outputs data from the data memory.

28. In regard to claim 14,

a. Okado discloses the data processing apparatus according to claim 10,

b. Okado does not disclose wherein said instruction memory includes a plurality of instruction memory banks, wherein said memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout to carry out a pipeline process when fetching an instruction from said plurality of instruction memory banks.

c. Hennessy has disclosed on pages 361-363 the use of memory banks for memory systems. Page 362 shows that one memory bank initiation or read is completed per clock cycle. The pages show that when reading from multiple banks, one bank is read from while the other is then selected in a generated cycle so that in the next generated cycle that bank is read from.

d. Page 361 of Hennessy shows that multiple memory banks allow for producing or accepting one word fetched or stored per clock cycle, which is faster than using one memory bank. This ability to speed up memory transfers would have motivated one of ordinary skill in the art to modify the design of Okado to use multiple memory banks in the instruction memory.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Okado to implement a plurality of memory banks in the instruction memory system as taught by Hennessy so that transfers of the memory are sped up.

29. In regard to claim 15, Okado in view of Hennessy discloses the data processing apparatus according to claim 14, wherein said instruction memory further comprises a first bank select circuit decoding an address including a low order address to generate chip select signals of said plurality of instruction memory banks so that a different instruction memory bank of said plurality of instruction memory banks is accessed when instructions at continuous addresses are accessed. It is inherent that if two instructions are stored at two memory addresses separated by the border of memory banks, that the memory bank must be switched to access the second instruction and that the low order address would play a role in chip-selecting the bank since it gives the border address of the bank.

30. In regard to claim 16,

a. Okado discloses the data processing apparatus according to claim 10,

b. Okado does not disclose wherein said data memory includes a plurality of data memory banks, wherein said memory operation unit generates a pipeline cycle corresponding to selection of a data memory bank and a pipeline stage corresponding to data access to carry out a pipeline process when said plurality of data memory banks are accessed.

c. Hennessy has disclosed on pages 361-363 the use of memory banks for memory systems. Page 362 shows that one memory bank initiation or read is

completed per clock cycle. The pages show that when reading from multiple banks, one bank is read from while the other is then selected in a generated cycle so that in the next generated cycle that bank is read from.

d. Page 361 of Hennessy shows that multiple memory banks allow for producing or accepting one word fetched or stored per clock cycle, which is faster than using one memory bank. This ability to speed up memory transfers would have motivated one of ordinary skill in the art to modify the design of Okado to use multiple memory banks in the data memory.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Okado to implement a plurality of memory banks in the data memory system as taught by Hennessy so that transfers of the memory are sped up.

31. In regard to claim 17, Okado in view of Hennessy discloses the data processing apparatus according to claim 16, wherein said data memory further comprises a second bank select circuit decoding an address including a high order address to generate chip select signals of said plurality of data memory banks in order to divide said plurality of data memory banks into two different regions. It is inherent that a higher order address will divide a memory bank into two sections. The highest bit of a memory address that switches within a memory bank indicates two section of that bank.

32. In regard to claim 18, Okado in view of Hennessy discloses the data processing apparatus according to claim 17, wherein said second bank select circuit decodes an address including a low order address to generate a chip select signal of said plurality of data memory banks so that a different data memory bank in said plurality of data

memory banks is accessed when data at continuous addresses in said two different regions are accessed. It is inherent that if two instructions are stored at two memory addresses separated by the border of memory banks, that the memory bank must be switched to access the second instruction and that the low order address would play a role in chip-selecting the bank since it gives the border address of the bank.

33. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okado in view of Watanabe (5,214,786).

34. In regard to claim 19,

a. Okado discloses the data processing apparatus according to claim 10,

b. Okado does not disclose wherein said memory operation unit saves a plurality of registers including said dedicated register and switches a task in a task switch operation.

c. Watanabe has disclosed in the abstract that registers are selectively saved on a task switch.

d. The abstract as well as the Summary then shows that by selectively saving registers on a task switch, critical information is stored so a switch back may start immediately and the saving portion is done faster. This ability to save critical information quickly would have motivated one of ordinary skill in the art at the time of invention to modify the design of Okado to include register saving on task switches as taught by Watanabe.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Okado to implement the register saving technique on a task switch taught by Watanabe so that critical information is quickly saved.

Conclusion

35. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents have been cited to further show the art with respect to loop execution.

US Pat No 6,125,440 to Osovets teaches storing repeated instructions in registers for faster fetching.

US Pat No 4,626,988 to George shows a buffer for storing repeated instructions for later fetching.

US Pat No 5,579,493 to Kiuchi discloses a system with repeat control circuitry for locally storing repeated instructions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
May 28, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100